Integration and optimization of ferroelectric 1T-1C FeMFET cells into a 8k-bit memory array

A.Viegas[1], R. Hoffmann[1], D. Lehninger[1], A. Sünbül[1], N.K.Yadav, K. Seidel[1*], J. Barbot[2], K. Bernert[2,] S.Thiem[2]

[1]*Fraunhofer IPMS, Center Nanoelectronic Technologies CNT, 01109 Dresden, Germany*

[2]*X-FAB Dresden GmbH and Company KG, Dresden, Germany*

Ferroelectric hafnium oxide has shown promising results in the field of memory applications due to its low power consumption, high operational speed, scalability and compatibility in the CMOS technologies [1]. However, when integrated into larger memory arrays, retention reliability continues to be a major challenge. In this paper, we show the integration of a 1T1C (1 transistor, 1 capacitor) memory bit cell (FeMFET) into an 8k bit array, fully integrated on 200 mm wafer in an 180 nm CMOS technology. The metal-ferroelectric-metal capacitor (MFM) is fabricated in the back end of line between metal lines M2 and M3, and connected to the gate of a standard transistor fabricated in the front end of line. The MFM capacitor and single FeMFET cell has been optimized in our previous publications [2],[3], that showed a superlattice approach for HZO layers in the MFM and the area ratios of the 1T and 1C have been adjusted for high memory window (MW) as well as reasonable switching voltage in the FeMFET cells. Here, we tune and optimize the parameters required for successful operation of the array, including wake up cycling, switching voltage optimization, inhibit optimization and pulse width variations. The array consists of 32 word lines (WL) and 256 bit lines (BL) paired along with 256 select lines (SL) arranged in cross bar structure as shown in [4], along with control circuitry. The endurance characteristics and retention characteristics of the array have been tested with the optimized parameters. Figure 1 shows the schematic of the FeMFET cell operation and the MW extraction. A memory window of 0.8V was achieved for cycling up to 10^5 endurance cycles over 512 cells, as seen in figure 2a. The array was also tested for retention schemes that involved writing solid and checkered patterns into the bitcells and reading them out at regular intervals of time. The patterns are clearly visible after being stored for more than 1 hour, seen in figure 2b. The current results are an improvement over the previous generation of FeMFET bitcells, as among enhanced operation conditions the materials of MFM devices were optimized and the MFM devices are integrated closer to the transistors.

References

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* Corresponding author: konrad.seidel@ipms.fraunhofer.de

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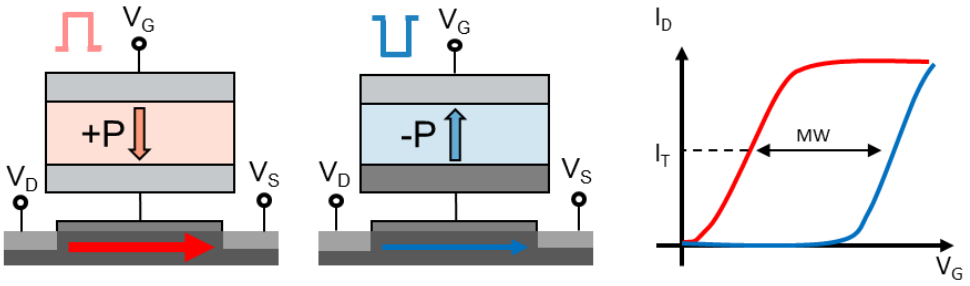

Figure 1: Schematic showing the operation of a single FeMFET cell. A positive pulse applied to the gate results in the programmed or low V_t (LVT) state, the negative pulse constitutes the erase/ high V_t (HVT) state. The difference is the memory window (MW), as measured in the drain current (I_D) vs. gate voltage (V_G) plot on the right.

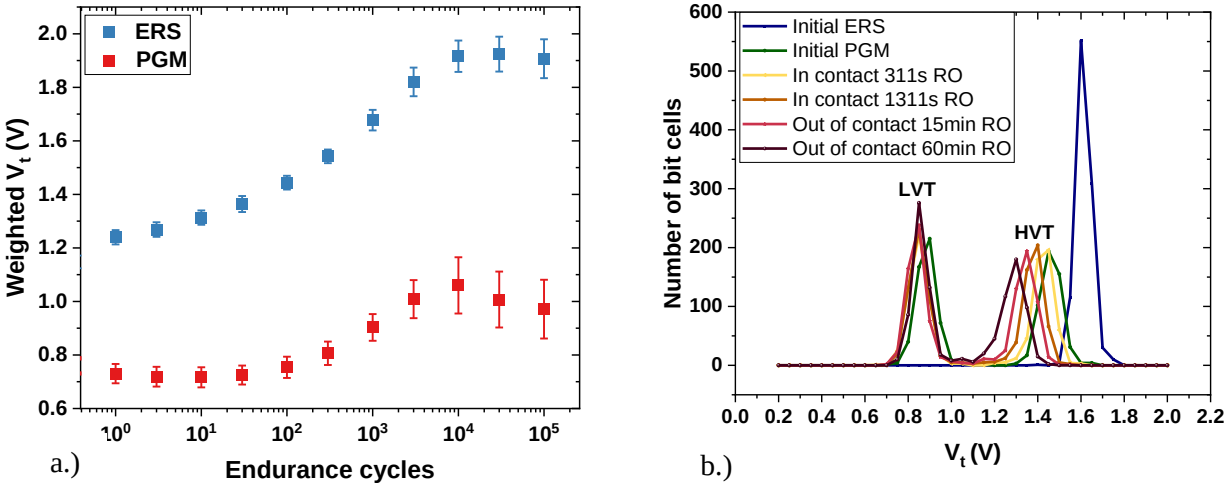

Figure 2a: Memory array characterization results of endurance cycling with no degradation and low variability of up to 100 k cycles. Weighted V_t refers to the V_t values over 512 bitcells. b.) Initial retention characteristics for a solid pattern, showing clear memory window between the LVT and HVT states, when measured in contact and out of contact readouts (RO). In contact refers to the array being probed, while waiting for readout. Out of contact refers to, no probes on the device while waiting for readout.